REMARKS

This application is under final rejection. Applicant has presented arguments below that Applicant believes should render the claims allowable. In the event, however, that the Examiner is not persuaded by Applicant's arguments, Applicant respectfully requests that the Examiner enter the amendments to clarify issues upon appeal.

In response to the Final Action mailed March 23, 2005, Applicant respectfully requests reconsideration in view of the following remarks.

Claims 1-15 were pending. Claims 6, 9 and 13 have been amended. Claims 10 and 11 have been cancelled. The specification has been amended to correct a typographical error. Independent claim 9 has been amended to incorporate the limitations of cancelled dependent claims 10 and 11, and, therefore, no new issues are raised with respect to the amendment to claim 9. Claims 6 and 13 were each amended to correct an informality. No new matter has been added. Accordingly, claims 1-9 and 12-15 remain pending.

I. The § 103 Rejections

Claims 1-15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,260,087 ("Chang1") in further view of and U.S. Patent No. 6,173,419 ("Barnett") and U.S. Patent No. 5,687,325 ("Chang2"). Applicant respectfully traverses.

Claim 1 recites an application specific integrated circuit (ASIC) that includes a standard cell having a plurality of logic functions. The ASIC further includes a field programmable gate array (FPGA) function including a debug client that observes a plurality of internal signals from the plurality of logic functions.

A potential advantage of such an ASIC is that the debug client (associated with the FPGA function) can be used to observe and, therefore, accordingly manipulate internal signals of the standard cell (specification p. 3, lines 6-12; p. 5, lines 4-6).

A. Chang1 Fails To Disclose an FPGA Function having a Debug Client That Observes a Plurality of Internal Signals From Logic Functions of a Standard Cell as recited in Claim 1

Chang1 discloses an ASIC that includes at least one non-programmable, hardware functional block and a programmable logic block (PLB 26) (see Abstract). In particular, the PLB 26 can be electrically programmed to perform at least one function that complements a function performed by the non-programmable functional block. The Examiner recognizes that Chang1 fails to disclose an FPGA function that includes a debug client. The Examiner, however, asserts that this limitation, as well as further limitations absent from Chang1 and recited in claim 1, are disclosed by Barnett and Chang2.

B. Barnett Fails To Disclose an FPGA Function having a Debug Client That Observes a Plurality of Internal Signals From Logic Functions of a Standard Cell as recited in Claim 1

Barnett discloses an emulator to debug software operating on a target micro-controller in a target circuit environment (see Abstract). The emulator contains an FPGA that is programmed to contain an emulated target micro-controller, and an emulated monitoring circuit that monitors the operations of the emulated micro-controller (col. 2, ll. 11-16).

On page 3, of the Final Action mailed March 23, 2005, the Examiner asserts that Barnett discloses the observe function as recited in claim 1. Applicant respectfully disagrees.

Barnett fails to disclose an FPGA function having a debug client that observes a plurality of internal signals from logic functions of a standard cell (emphasis added). Instead, Barnett discloses an FPGA having debug circuitry that monitors only those signals internal to the FPGA *itself* (col. 2, ll. 31-33; col. 5, ll. 40-43; col. 6, ll. 19-24). That is, because Barnett's FPGA contains both the emulated target micro-controller *and* the emulated monitoring circuit, it necessarily follows that Barnett's emulated monitoring circuit monitors only those signals internal to the FPGA, and not internal signals from logic functions of a standard cell.

C. Chang2 Fails To Disclose an FPGA Function having a Debug Client That Observes a Plurality of Internal Signals From Logic Functions of a Standard Cell as recited in Claim 1

Chang2 discloses a general purpose field programmable gate array that is configurable to effect a specific digital logic circuit interconnection between fixed functional units within an Application Specific Field Programmable Gate Array (ASFPGA) (see Abstract; col. 3, ll. 32-37). The Examiner does not cite Chang2 as disclosing an FPGA function having a debug client that observes a plurality of internal signals from logic functions of a standard cell. Nevertheless, Chang2 (as with Chang1 and Barnett) fails to disclose an FPGA function having a debug client that observes a plurality of internal signals from logic functions of a standard cell.

D. The claim has limitations not taught by the references

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

Chang1, Barnett and Chang2 fail to disclose an FPGA function having a debug client that observes a plurality of internal signals from logic functions of a standard cell. Consequently, the

combination of Chang1, Barnett and Chang2 cannot render claim 1 obvious, and the Examiner has not made a *prima facie* showing of obviousness.

E. No Motivation To Combine Chang1 and Barnett

As recognized by the Examiner, the test for combining references is what the references as a whole would have suggested to one of ordinary skill in the art. *In re Sheckler*, 168 USPQ 716 (CCPA 1971). However, prior art references must be considered in their entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983).

As discussed above, Chang1 discloses an ASIC including a PLB 26 that can be electrically programmed to perform at least one function that complements a function performed by a non-programmable functional block. The PLB 26, however, does not include FPGA technology. Instead, the PLB 26 "employs Programmable Logic Device PLD technology because it is *simpler* to use than FPGA technology" (col. 7, ll. 56-61). Moreover, Chang1 further discloses that FPGAs are *alternatives* to ASICs, and that FPGAs prove excessively expensive and cannot, in general, provide a circuit density and/or performance comparable to ASICs (col. 2, ll. 24-44). Based on these portions, Applicant respectfully submits that Chang1, therefore, teaches away from combining Barnett's FPGA emulator – or any FPGA function – with the ASIC as disclosed in Chang1.

F. Proposed Combination Would Change Principle Of Operation Of Barnett

"If [a] proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious." *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959).

As discussed above, Barnett's FPGA emulator includes both an emulated target micro-controller and an emulated logic circuit. In particular, the emulated logic circuit permits a software engineer to execute software code instructions to monitor activities within the emulated target micro-controller (col. 6, ll. 19-24).

Assuming, *arguendo*, that the principles of Chang1's ASIC and Barnett's FPGA emulator could be combined to yield an ASIC with a debug function, Applicant submits that further modifying Barnett's FPGA to observe and manipulate signals outside of Barnett's FPGA emulator would substantially alter a principle of operation of Barnett's FPGA emulator – which is to specifically monitor only those signals internal to the FPGA emulator *itself*, as discussed above (emphasis added). Moreover, Barnett does not provide any teachings or suggestions as for how the software code instructions (for monitoring activities within the emulated target micro-controller) could be modified to observe and manipulate signals outside of the FPGA emulator – e.g., internal signals from logic functions of a standard cell.

For at least these reasons, Applicant submits that claim 1, and the claims that depend therefrom, are in condition for allowance.

G. Dependent Claim 3

Dependent claim 3 incorporates the limitations of claims 1 and 2, and further recites that the debug client function further observes and manipulates at least one of the plurality of logic functions on the standard cell.

In rejecting claim 3, the Examiner applied the same arguments that was applied to claim 1. Applicant respectfully traverses.

As discussed above, the general FPGA (48) of Chang2 is configurable to provide specific digital interconnections between various fixed functional units (*see* col. 5, line 66 – col. 6, line

4). Chang2 further discloses that the general FPGA 48 *itself* can be configured to perform functions in addition to those provided by fixed functional units 12-26 (FIG. 1; col. 6, ll. 19-34). Nevertheless, providing specific digital interconnections between various functional units, and configuring the general FPGA 48 *itself* to perform functions does not manipulate in any way logic functions associated with the fixed functional units. Consequently, Chang2 fails to disclose manipulating at least one of the plurality of logic functions on the standard cell, as recited by claim 3. For at least these reasons, Applicant respectfully submits that claim 3 is allowable.

H. Other Independent Claims

Claim 9, as amended, incorporates limitations similar to those of claim 1. Claim 9, and the claims that depend therefrom, are also allowable over the combination of Chang1, Barnett, and Chang2 for reasons corresponding to those set forth with respect to claim 1.

In view of the foregoing, it is submitted that the claims 1-9 and 12-15 are allowable over the cited references, and are in condition for allowance. Should any unresolved issues remain, the Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,
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